

APPLICATION  
  
FOR  
  
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TITLE:            VARIABLE LEVEL MEMORY

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VARIABLE LEVEL MEMORY

Background

This invention relates generally to memory devices and particularly to memory devices with a multi-level cell  
5 architecture.

A multi-level cell memory is comprised of multi-level cells, each of which is able to store multiple charge states or levels. Each of the charge states is associated with a memory element bit pattern.

10 A flash EEPROM memory cell, as well as other types of memory cells, is configurable to store multiple threshold levels ( $V_t$ ). In a memory cell capable of storing two bits per cell, for example, four threshold levels ( $V_t$ ) are used. Consequently, two bits are designated for each threshold  
15 level. In one embodiment, the multi-level cell may store four charge states. Level three maintains a higher charge than level two. Level two maintains a higher charge than level one and level one maintains a higher charge than level zero. A reference voltage may separate the various  
20 charge states. For example, a first voltage reference may separate level three from level two, a second voltage reference may separate level two from level one and a third reference voltage may separate level one from level zero.

A multi-level cell memory is able to store more than one bit of data based on the number of charge states. For example, multi-level cell memory that can store four charge states can store two bits of data, a multi-level cell  
5 memory that can store eight charge states can store three bits of data, and a multi-level cell memory that can store sixteen charge states can store four bits of data. For each of the N-bit multi-level cell memories, various memory element bit patterns can be associated with each of the  
10 different charge states.

The number of charge states storable in a multi-level cell, however, is not limited to powers of two. For example, a multi-level cell memory with three charge states stores 1.5 bits of data. When this multi-level cell is  
15 combined with additional decoding logic and coupled to a second similar multi-level cell, three bits of data are provided as the output of the two-cell combination. Various other multi-level cell combinations are possible as well.

20 The higher the number of bits per cell, the greater the possibility of read errors. Thus, a four bit multi-level cell is more likely to experience read errors than a one bit cell. The potential for read errors is inherent in the small differential voltages used to store adjacent  
25 states. If the stored data is potentially lossy, sensitive

data stored in relatively high-density multi-level cells may be subject to increased error rates.

In many applications, the nonvolatile memories store a large amount of data that is tolerant to a small number of  
5 bit errors. Applications may also have a small amount of data that is not tolerant to bit errors. Examples of such applications may include control structures, header information, to mention a few examples. These typical applications, where a relatively small amount of the  
10 overall storage requires higher fidelity, may include digital audio players, digital cameras, digital video recorders, to mention a few examples.

Thus, there is a need for a way to store a large amount of data in dense multi-level cells while ensuring  
15 that sensitive data is stored in a fashion that sufficiently reduces the possibility of read errors.

#### Brief Description of the Drawings

Figure 1 is a block depiction of one embodiment of the present invention;

20 Figure 2 is a depiction of a cell in accordance with one embodiment of the present invention;

Figure 3 is a depiction of another cell in accordance with another embodiment of the present invention;

Figure 4 is a depiction of still another cell in  
25 accordance with one embodiment of the present invention;  
and

Figure 5 is a flow chart for software in accordance with one embodiment of the present invention.

#### Detailed Description

Referring to Figure 1, a processor 100 may be coupled  
5 through a bus 102 to a multi-level cell memory 104. The  
memory 104 contains an interface controller 105, a write  
state machine 106 and a multi-level cell memory array 150.  
The processor 100 is coupled by the bus 102 to both the  
interface controller 105 and the memory array 150 in one  
10 embodiment of the present invention. The interface  
controller 105 provides control over the multi-level cell  
memory array 150. The write state machine 106 communicates  
with the interface controller 105 and the memory array 150.  
The interface controller 105 passes data to be written into  
15 the array 150 to the state machine 106. The state machine  
106 executes a sequence of events to write data into the  
array 150. In one embodiment, the interface controller  
105, the write state machine 106 and the multi-level cell  
memory array 150 are located on a single integrated circuit  
20 die.

Although embodiments are described in conjunction with  
a memory array 150 storing one, two or four bits per cell,  
any number of bits may be stored in a single cell, for  
example, by increasing the number of threshold levels,  
25 without deviating from the spirit and scope of the present  
invention. Although embodiments of the present invention

are described in conjunction with a memory array 150 of flash cells, other cells such as read only memory (ROM), erasable programmable read only memory (EPROM) conventional electrically erasable programmable read only memory  
5 (EEPROM), or dynamic random access memory (DRAM), to mention a few examples, may be substituted without deviating from the spirit and scope of the present invention.

Referring to Figure 2, a cell may include only one bit  
10 of data at the first and last states of the cell. In the embodiments shown in Figures 2, 3 and 4, the actual storage of data is indicated by an X and empty states are indicated by dashes. A similarly sized cell, shown in Figure 3, may store two bits per cell at every fifth level within the  
15 cell. Likewise, as shown in Figure 4, the same sized cell may store four bits per cell using every single state or level of the sixteen available states in this example.

Thus, in some embodiments of the present invention, the number of bits per cell may be changed to increase the  
20 fidelity of the stored data. Thus, if density is more important than fidelity, the scheme shown in Figure 4 or other higher density schemes may be utilized. Conversely, when fidelity is more important, the data may be spread in the cell, decreasing the density per cell and increasing  
25 the number of cells required to store all of the data. With wider spacing between the states that are utilized,

the integrity of the data storage will be improved. This is because it is easier to discern the differential voltage between significantly nonadjacent levels. In fact, the greater the distance between the levels, the easier it is to discern a differential voltage.

Thus, in the embodiment shown in Figure 2, only two levels are used, and in the embodiment shown in Figure 3, four levels are used. In the embodiment shown in Figure 4, all sixteen levels are utilized in accordance with some embodiments of the present invention.

Thus, in some embodiments, data may be stored in varying numbers of bits per cell depending on the type of data involved. Thus, some data may be packed closely as indicated for example in Figure 4 and other data may be spread farther apart, requiring additional numbers of cells to complete the data storage.

Thus, turning to Figure 5, the write algorithm 122, which may be implemented in software or hardware, initially identifies the number of bits per cell. The number of bits per cell may be derived from information included with the data indicating the desired fidelity. Based on the number of bits per cell, the packing of bits into each given cell may be adjusted. Thus, in some cases, denser packing may be utilized, for example as shown in Figure 4, and in other cases, looser or more spread apart packing may be utilized as shown in Figure 2. Once the number of bits per cell has

been determined as indicated in block 124, the packing of bits into each cell is adjusted as indicated in block 126. Finally the bits are written to the cells as indicated in block 128. The number of bits per cell may be changed on  
5 the fly from cell to cell.

The read process simply reverses the flow, ignoring the missing levels, and simply reading the actual data out of each cell. The spread apart data may then be repacked into a continuous data string.

10 While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall  
15 within the true spirit and scope of this present invention.

What is claimed is: